surface 22 of substrate 20 as well as adjacent to and elevationally above source/drain (S/D) regions 24. In accordance with embodiments of the present invention, gate dielectric 60 encompasses metal-containing dielectric layers 45 and 55 (Fig. 2) where such layers are formed as described above and subsequently patterned using any of the appropriate methods for patterning a gate electrode 80 and dielectric 60. S/D regions 24 and sidewall spacers 70 are also formed by appropriate methods. It will be understood that transistor 14 is a simplified transistor representation, and that more complex transistor structures are also encompassed by embodiments of the present invention. For example, in some embodiments, transistor 14 is a MOSFET having an gate dielectric layer 60 that has an equivalent oxide thickness (EOT) of 2 nm or less while having an actual thickness of as much as about 6 nm. Such an advanced MOSFET can also have a gate length of about 0.25 micron or less and be encompassed within an integrated circuit such as a dynamic random access memory (DRAM), static random access memory (SRAM) or any of the various other memory integrated circuits. Transistor 14 can also encompass a gate dielectric layer 60 that has an EOT of greater than 2 nm and a gate length of more than 0.25 micron. --.